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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/672,395	09/28/2000	Paul Lap Tak Cheng	0325.00370	8271

21363 7590 09/14/2004

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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	8

DATE MAILED: 09/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/672,395	Applicant(s) CHENG ET AL.	
	Examiner James K. Trujillo	Art Unit 2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/25/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file:

2. Claims 1-21 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Applicant's arguments with respect to claim 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims16 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16 recites the limitation "first signals" in lines 4-5 of the claim. There is insufficient antecedent basis for this limitation in the claim. It appears that the applicants may be referring to one or more first control signals, however it seems that one or more clock signal seems be more appropriate. The examiner cannot determine which set of signal the applicants are referring to.

7. As to claim 17, it dependent upon claim 16 and is therefore rejected for the same reasons as claim 16.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1-2, 7-8, 14, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Poisner et al., U.S. Patent 6,269,443.

10. As to claim 1, Poisner teaches an apparatus comprising:

a. a first circuit (clock frequency multiplier indicator circuit) configured to change a frequency of one or clock signals (for processor operation) in response to one or more first control signals (generated within the processor) [figures 2, 3, col.3 lines 45-50 and col. 3 line 61 through col. 4 lines 8-14];

b. a second circuit (processor 210) configured to generate said one or more first control signals (the processor is able to adjust the values in the clock frequency multiplier circuit thus using control signals) [col. 4 lines 8-10] and a second control signal (signal to determine if a first instruction fetch that addresses address the non-volatile memory is used as a control signal) [col. 3 lines 17-19];

c. a third circuit (processor failure detection circuit 284) configured to generate a first reset signal (reset) in response to either said second control signal (the fetching of an address) or a predetermined time period expiring (timer expires when processor does not reset the timer) [col. 3 lines 20-23 and col. 3 line 61 through col. 4 line 7].

11. As to claim 2, Poisner taught the apparatus according to claim 1, as described above. Poisner further teaches wherein said one or first control signals (signals from processor) are configured to program said frequency of one or clock signals [col. 4 lines 1-10]. Specifically, the processor of Poisner adjusts the values in the clock frequency multiplier indicator circuit. The values in the clock frequency multiplier circuit are used to establish the frequency of operation of the processor.

12. As to claim 7, Poisner taught the apparatus according to claim 1, as described above. Poisner further teaches wherein said second circuit (processor) is further configured to generate a third control signal (signal to reset timer) and said predetermined time is started (timer is reset) in response to said third control signal [col. 3 lines 22-23].

13. As to claim 8, Poisner taught the apparatus according to claim 1 as described above. Poisner further teaches wherein said third circuit (processor failure detection unit) further comprises a watch dog timer circuit configured to measure said predetermined time period in response to said third control signal [col. 3 lines 17-25]. Specifically, Poisner teaches a timer (within the processor failure detection unit) that measures the time period when the processor last communicated with the processor failure detection unit using a timer. The time is reset when communications have been established. If communications has not been established within the

predetermined time period a failure is detected. These are the functions of a watchdog timer as will be appreciated by those of ordinary skill in the art.

14. As to claim 14, Poisner taught the apparatus according to claim 1 as described above. Poisner further teaches wherein said third circuit (processor failure detection unit) is further configured to generate a second reset signal in response to the expiration of said predetermined time period [col. 3 line 17-25 and figure 3]. Specifically, Poisner teaches that two reset signals may be initiated. The first reset signal is if the processor fails to perform a first instruction fetch. The second reset signal is if the processor fails to reset a timer.

15. As to claim 18, Poisner teaches an apparatus comprising:

a. means (clock frequency multiplier indicator circuit) for changing a frequency of one or more clock signals in response to one or more first control signals [figures 2, 3, col.3 lines 45-50 and col. 3 line 61 through col. 4 lines 8-14];

b. means (processor 210) for generating one or more first control signal and a second control signal [col. 4 lines 8-10 and col. 3 lines 17-19];

c. means (processor failure detection circuit 284) for generating a reset signal in response to either said second control signal or a predetermined time period [col. 3 lines 20-23 and col. 3 line 61 through col. 4 line 7].

Claim Rejections - 35 USC § 103

16. Claims 3-4 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al., U.S. Patent 6,269,443 in view of Mote, Jr., U.S. Patent 5,630,110 (hereinafter Mote, previously cited reference).

17. As to claim 3, Poisner taught the apparatus according to claim 1 as described above. Poiser does not expressly address wherein said first clock signals are generated by one or phase lock loop circuits. Poisner only teaches that the clock signals must be generated.

Mote teaches wherein one or more first clock signals are generated by one or more phase lock loop circuits [figures 1 and 2]. Mote teaches a system, similar to that of Poisner, that uses control signals to control the frequency of a processor. It appears that the feature of using one or more phase lock loops in Mote provide advantage of being programmable to allow many frequencies to be generated from a single oscillating source while providing a stable clock frequency.

It would have been obvious to one of ordinary skill in the art, having the teachings of Poisner and Mote before them at the time the invention was made, to use the one or more phase lock loop circuits as taught by Mote for the generation of clock frequencies in as disclosed by Poisner as the phase lock loop circuits taught by Mote is a known suitable for the use as the generation of frequency of Poisner.

One of ordinary skill in the art would have been motivated to make this modification in order provide stable clock frequencies with the advantage of being programmable to allow many frequencies to be generated from a single oscillating source in view of the teachings of Mote.

18. As to claim 4, Poisner together with Mote taught the apparatus according to claim 3 as described above. Poiser teaches using one or more control signals to control signal are configured to program a frequency of operation. Mote teaches wherein the one or more control signals are configured to program at least one of said one or phase lock loop circuits.

19. As to claim 19, Poisner teaches a method for recovering from a processor hang due to over-clocking comprising the steps of:

a. changing a frequency of a clock signal in response to one or more first control signals [col. 4 lines 1-19];

b. generating said one or more first control signals and a second control signal, wherein said processor is reset in response to said second control signal when said frequency is changed [figure 3and col. 4 lines 1-7]; and

c. detecting whether said processor hangs in response to said frequency change (timer expires when processor does not reset the timer) [col. 3 lines 17-25].

Poisner does not expressly disclose the recovery is in a phase lock loop circuit. The system of Poisner is direct toward changing the clock frequency of a CPU.

Mote teaches using a phase lock loop to supply the clock frequency of CPU [figure 2]. The system of Mote is similar to that of Poisner in that both systems change the clock frequency of a CPU based on control signals. It appears that the phase lock loop in Mote provide the advantage of being easily able to programmably change the clock frequency that is concise and reliable.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the phase lock loop as taught by Mote for the clock generation circuit as taught by Poisner as the phase lock loop taught by Mote is a known suitable implementation as the clock generation circuit in Poisner.

One of ordinary skill in the art would have made this combination in order to concisely and reliably change the clock frequency in Poisner in view of the teaching of Mote.

20. As to claim 20, Poisner together with Mote taught the method according to claim 19. Poisner further teaches when said processor hangs changing said frequency of said clock signal to a fail-safe frequency and resetting said processor [col. 4 lines 1-7]. Specifically, Poisner teaches reducing the frequency to the lowest possible (fail-safe frequency) at which the processor will operate.

21. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al., U.S. Patent 6,269,443 in view of Gupta et al., U.S. Patent 5,996,083.

22. As to claim 5, Poisner taught the apparatus according to claim 5 as described above. Poisner fails to discuss wherein said one or more clock signals are generated using a divider network. Poisner only teaches that the microprocessor receives control signals to generate a clock signal.

Gupta teaches wherein one or more clock signals are generated using a divider network [figures 3, 4 and col. 6 lines 29-39]. Gupta teaches a computer system similar to that of Poisner having a CPU with a clock signal generating circuit. Gupta further teaches that the clock signal is divided and distributed by a clock divider network throughout the processor. In Gupta, similar to Poisner, the clock divider network receives a control signal to adjust the clock frequency throughout the processor. It appears that feature of using a clock divider network would allow the clock signal to be controlled and distributed throughout the processor minimizing skew and delay.

It would have been obvious to one of ordinary skill in the art, having the teachings of Poisner and Gupta before him at the time the invention was made to modify the processor as disclosed by Poisner to include a divider network as taught by Gupta in order to obtain clock frequency control.

One of ordinary skill in the art would have been motivated to make this modification in order to control and distribute the clock signal minimizing skew and delay in view of the teachings of Gupta.

23. Claims 6 and 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner et al., U.S. Patent 6,269,443 in view of Allen et al., U.S. Patent 5,233,613.

24. As to claim 6, Poisner taught the apparatus according to claim 1 as described above. Poisner teaches using a predetermined time period to determine when to issue a reset but does not explicitly disclose wherein said predetermined time period is programmable.

Allen teaches using a predetermined time period that is programmable [col. 1 lines 51-66]. Allen further teaches a system similar to that of Poiser in that Allen also uses the predetermined time period to monitor a processor and reset the processor if the processor fails to communicate to the timer [col. 1 lines 17-26]. Allen further teaches that his time provides the advantage of being programmable and highly reliable (immune from ESD, power glitches and errant software).

It would have been obvious to one of ordinary skill in the art, having the teachings of Poisner and Allen before them at the time the invention was made, to substitute the timer as disclosed by Poisner with timer as taught by Allen to obtain a programmable time period. One

of ordinary skill would have made this substitution in order to provide a programmable time period that is highly reliable in view of the teaching of Allen.

25. As to claim 9, Poisner taught the apparatus according to claim 1 as described above. Poisner further teaches wherein said first reset signal is presented to a reset input of said processor (reset 201). Poisner does not expressly disclose wherein one of said one or more clock signals are presented to a clock input of a processor. Specifically, Poisner appears to disclose wherein his processor uses an internal clock. Poisner, however, teaches that his invention may use other types of processors.

Allen teaches a system wherein one or more clock signals is presented to a clock input of a processor. The system of Allen teaches is similar to that of Poisner in that both systems generate a reset in response to a predetermined time period expiring [col. 1 lines 17-26].

It would have been obvious to one of ordinary skill in the art, having the teachings of Poisner and Allen before them at the time the invention was made, to modify Poisner by incorporating the processor and system clock of Allen into the system Poisner as the system clock and processor of Allen is a known suitable substitute as the processor of Poisner. Furthermore, Poisner suggests that other types of processors may be incorporated as embodiments within his invention. One of ordinary skill in the art would have made the modification because the advantages [col. 2 lines 3-7] of Poisner would be gained in a system using a separate CPU and system clock.

26. As to claim 10, Poisner together with Allen taught the apparatus according to claim 9, as described above. Poisner further teaches that the one or more first control signals are generated using a number of instructions executed by said processor [col. 4 lines 8-10].

27. As to claim 11, Poisner together with Allen taught the apparatus according to claim 10, as described above. Poisner further teaches wherein said instructions contained in computer readable medium. This is because the processor executes the instruction necessitates that the instructions are contained in a computer readable medium.

28. As to claim 12, Poisner together with Allen taught the apparatus according to claim 10, as described above. Poisner further taught wherein said instructions are part of a basic input output system (BIOS) routine [col. 4 lines 20-30 and figure 3]. Poisner discloses that the actions of the apparatus are initiated with strapping signals just subsequent to a reset signal. Further the actions take place before normal system operation. One of ordinary skill would recognize that strapping suggests using the BIOS for the strapping signals such as in bootstrapping the system.

29. As to claim 13, Poisner together with Allen taught the apparatus according to claim 90, as described above. Poisner further taught wherein said predetermined time period expires only when said processor hangs [col. 3 lines 20-25]. It is interpreted that the processor hangs when the processor fails to reset the timer.

30. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner as applied to claim 1 above, and further in view of I^2C Bus specification (submitted in IDS, hereinafter "the I^2C Bus specification").

31. As to claim 15, Poisner taught the apparatus according to claim 1 described above. Poisner does not expressly wherein said circuit comprises an inter-integrated circuit interface circuit.

The I^2C Bus specification teaches using an I^2C Bus has many advantages [pages 4-6]. It would have been obvious to one of ordinary skill in the art at the time of the invention to Poisner by incorporating within his circuitry an inter-integrated (I^2C) interface circuit. An artisan would have made the modification because the I^2C Bus specification teaches that it is beneficial to use an I^2C bus for coordinating data and clock signals between buses. Using an I^2C Bus necessitates implementing an inter-integrated (I^2C) interface circuit, resulting in the claimed invention.

32. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner as applied to claim 1 above, and further in view of Finch et al., U.S. Patent 5,513,319 (previously cited).

33. As to claim 21, Poisner taught the apparatus according to claim 14 as described above. Poisner do not address wherein said first reset signal is configured to reset a processor and said second reset signal is configured to reset an entire system.

Finch teaches a first reset signal that is configured reset signal a processor (CPU) and a second reset signal that is configured to reset an entire system. In Finch if the processor is locked and cannot respond the entire system (PC system) is reset (restarted) using a fourth signal [col. 5 lines 53-65]. The system of Finch is similar to that of Poisner in that both systems are directed toward resetting portions of the system. It appears that the two types of reset signals in Finch provides the advantage of only requiring an entire system boot when necessary, thereby reducing time in booting only the processor if possible.

It would have been obvious to one of ordinary skill in the art, having the teachings of Poisner and Finch before them at the time the invention was made, to modify the issuing of the

reset signals of Poisner to determine if an entire system is to be reset or only the processor is to be reset as taught by Finch in order to obtain two types of reset signals. One of ordinary skill in the art would have been motivated to make this modification in order to reduce the time for booting when possible.

Allowable Subject Matter

34. Claim 16-17 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291 [new phone number may be in effect in mid October - (571) 272-3677]. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (703) 308-1159 [new phone number may be in effect in mid October - (571) 272-3670]. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James Trujillo
September 7, 2004

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